Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **VLSI design** Code: **C028611(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To understand the IC design aspects, basic fabrication steps.
2. To study the design rules & representation of circuits at lower level of abstraction.
3. To understand the layout design of few combinational and sequential circuits.
4. To study one of the HDL (hardware description language) for front end design.
5. To study internal structure of programmable logic devices.

UNIT I An Overview & Analysis of CMOS Integrated Circuits: Complexity and Design: Design Flow, VLSI Chip Types, Moore's Law; MOSFETs as Switch: FET Threshold Voltages, Pass Characteristics; Basic Logic Gates in CMOS: NOT Gate, NOR Gate, NAND Gate; Complex Logic Gates in CMOS: Structured Logic Design, XOR and XNOR Gates; Transmission Gate Circuits: Multiplexers, OR Gate, XOR/XNOR Gate. DC characteristics of the CMOS inverter, Switching Characteristics: Fall Time, Rise Time, Propagation Delay; Power Dissipation.

UNIT II Fabrication & Physical Design of CMOS Integrated Circuits: CMOS Layers; Designing FET Arrays; Basic Gate Designs; Complex Logic Gates; Euler Graph; Overview of Silicon Processing; Material Growth and Deposition; Lithography; CMOS Process Flow; CMOS Design Rules; Layout of Basic Structures: nWell, Active Areas, Doped Silicon Regions, MOSFETs, Active Contacts, Metal, Vias; Physical Design(Stick diagram &Layout Design) of Logic Gates: NOT, NAND & NOR.

UNIT III CMOS Subsystem Design: Schematic and Layout of CMOS Combinational Circuits: Full adder circuit, Multiplexer, Parity Generator, Schematic and Layout of CMOS Sequential Circuits: SR FlipFlop, JK Flip-Flop, & D Flip-Flop, 4x4 NOR based ROM Array, 4x4 NAND based ROM Array; Schematic of SRAM Schematic and operation of DRAM: 3-T DRAM 6-T DRAM;

UNIT IV Implementation Technology & Introduction to VHDL: Implementation Technology: CPLD Architecture, FPGA Architecture, LUT Design; Brief history of VHDL, Entity Declaration, Architecture Declaration, Modeling styles: Data Flow, Structural, Behavioral and Mixed Style. Assignment Statements, Select Signal Assignment, Conditional Signal Assignment, Component Declaration, Generate Statements, Concurrent and Sequential Assignment Statement, Process Statement, Case Statement. VHDL operators. VHDL programming of Multiplexer, Decoder, Encoder, Half Adder, Full Adder, 4-bit Adder, ALU.

UNIT V Sequential Logic Design using VHDL: VHDL Programming for D-Latch, SR Flip-Flop, JK Flip-Flop, T Flip-Flop& D Flip-Flop, Shift Registers, Synchronous Counter: UP counter, Down counter, BCD counter; Moore Finite State Machine for Sequence Detector, MOD counter & Serial Adder. Mealy

Finite State Machine for Sequence Detector, MOD counter & Serial Adder. Test Bench design for Half Adder, Full adder & D Flip-Flop.

Textbooks:

1. Introduction to VLSI Circuits and Systems: John P. Uyemura, John Wiley & Sons (Unit-I & II).
2. CMOS Digital Integrated Circuits: Analysis & Design; Sung-Mo Kang & Yusuf Leblebici, TMH, (Unit-III)
3. Fundamentals of Digital Logic with VHDL Design, Brown, TMH Pub. (Uni- IV & V)
4. VHDL Primer by J. Bhaskar, PHI(Unit-IV & V)

Reference Books:

1. CMOS VLSI Design: A Circuits and Systems Perspective by Weste, Pearson Education Pub.
2. Basic VLSI Design by Pucknell&Esharghian,3rd Ed., PHI Pub.
3. CMOS circuit design, layout and simulation by Jacob Baker, PHI

Course Outcomes:

1. Students are expected to understand CMOS fabrication details.
2. Students are expected to understand schematic, layout of combinational circuits.
3. Students are expected to understand schematic, layout of sequential circuits.
4. Students are expected to understand VHDL programming concepts.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Antenna & Wave Propagation** Code: **C028612(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To study uniform plane wave propagation in different media and wave polarization
2. To study guided wave propagation in metallic wave guides
3. To study radio wave propagation
4. To study the concept of radiation and analyze radiation characteristics of a current element and dipole
5. To study antenna fundamentals and antenna arrays: uniform and tapered and their design
6. To study some practical antennas like Rhombic, Loop, Yagi and microstrip antenna.

UNIT – I Waveguides: Wave propagation between two infinite parallel conducting plane: TE and TM modes; Properties of TE and TM modes, TEM waves; Rectangular and Circular waveguides: TE and TM modes, dominant modes, characteristics: attenuation and phase constants, phase and group velocities, cut-off wavelengths and frequencies, guide wavelength, field pattern and wave impedance.

UNIT – II Wave Propagation: Sky wave, surface wave and space wave; Ionospheric propagation-refractive index at high frequencies; Mechanism of radio wave bending, critical frequency; effect of earth's magnetic field; Effective dielectric constants and conductivity, MUF, skip distance, optimum working frequency; Multihop propagation; Ionoshperic abnormalities; Troposhperic propagation, field strength of troposhperic wave; Effect of earth's curvature and dielectric constant; Troposhperic scatter and Duct propagation.

UNIT – III Antennas and Radiation: Electromagnetic radiation; Retarded potentials; Short electric dipole, radiation from a small current element, radiated power and radiation resistance; Radiation from a half wave dipole and its radiation resistance; Isotropic radiator; radiation pattern; Radiation Intensity; Antenna Gain: directive gain and power gain; Antenna directivity; Effective length and effective aperture of antennas; Beam width; Bandwidth; Beam area; FBR, Self impedance of antennas, Antenna efficiency; Reciprocity theorem and its application.

UNIT – IV Antenna Arrays and their design: Various form of array: broadside, end fire, collinear and parasitic arrays; Arrays of two isotropic point sources; Principle of pattern multiplication; Linear arrays with 'n' isotropic point sources of equal amplitude and spacing: broadside and end fire case; Tapering of arrays: Binomial and Dolph Tchebysceff array.

UNIT – V Practical Antennas: Effect of earth on antenna performance; Grounded and ungrounded antennas; Antenna top loading and tuning; Resonant and non-resonant antennas; Beverage antenna; Tower radiator; Long-wire antenna; V-antenna; Rhombic antenna; Loop antenna and Adcock antenna; Yagi antenna; Log periodic antenna; Horn and Microstrip antenna.

Name of Text Books:

1. Engineering Electromagnetic, William H. Hyat, Jr. John A. Buck 7th Ed. TMH, 2006. (Unit: I)
2. Antennas and Wave Propagation, K. D. Prasad, Satya Prakashan, 3rd Ed., 2001.(Unit: I, II, III,IV &V)

Name of Reference Books:

1. Antenna Theory, Balanis, 2nd Edition, John Wiley & Sons, 2003.
2. Antenna and Wave Propagation, R.L. Yadava, PHI, 2011.
3. Antenna and Wave Propagation, G. S. N. Raju, , 5th Impression, Pearson, 2011.
4. Antennas and Radio Propagation, R.E. Collins, McGraw-Hill, 1987.
5. "Antennas", John D. Kraus and Ronalatory Marhefka, Tata McGraw-Hill Book, 2002.

Course outcome:

1. Students will be able to understand the guided and unguided wave propagation.
2. Students will acquire knowledge of Basic antennas, their radiation and characteristics.
3. Students will knowledge of antenna arrays and their design.
4. Students will able to understand some different practical antennas.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Digital Signal Processing** Code: **C028613(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objective:

- To Study the Basic Mathematical Techniques needed for analysis of discrete time Signals and Systems.
- To Study the Various Digital Filter Design Techniques.
- To Study the Multirate Digital Signal Processing Techniques.

UNIT I Analysis of Discrete Time Signals and Systems: Discrete Fourier analysis, Classification, Discrete Time Fourier Transform (DTFT) & its properties, Inverse DTFT. Discrete Fourier Transform (DFT) & its Properties, Inverse DFT. Fast Fourier Transform, Properties, Types of FFT, N-point Radix-2 FFT, Inverse FFT. Discrete Linear Convolution, Circular Convolution, Fast Convolution, Frequency Response of LTI system using Discrete Fourier Analysis.

UNIT II Implementation of Discrete-time Systems: Structures for the Realization of discrete-time systems, Structures for FIR systems: Direct, Cascade, Frequency Sampling & Lattice structures. Structures for IIR systems: Direct, Signal Flow Graphs & Transposed, Cascade, Parallel, Lattice & Lattice-Ladder structures.

UNIT III FIR Filter Design: Symmetric and Anti-symmetric FIR filters, FIR Filter design by window method (Rectangular, Bartlett, Hamming, Hanning, Blackman and Kaiser window), Frequency Sampling method, Optimum approximation of FIR filters, Design of FIR differentiators, Design of Hilbert transformers.

UNIT IV IIR Filter Design: Design of Discrete-time IIR filters from Continuous-time Filters: Filter design by Impulse invariant and bilinear transformation method: Butterworth, Chebyshev & Elliptic approximation Filter, Frequency transformation.

UNIT V Multirate Digital Signal Processing: Introduction, Decimation, Interpolation, Sampling rate conversion by rational factor, Filter design and implementation for sampling rate conversion: Direct form FIR digital filter structure, Polyphase filter structure, Time varying digital filter structure, Sampling rate conversion by an arbitrary factor.

Text Books:

1.Discrete Time Signal Processing by A.V. Oppenheim, R. W. Schafer, & John R. Buck, , 2nd Edition, Prentice Hall, 1999. (Unit I, Unit II, Unit III, Unit IV)

2. Digital Signal Processing: Principles, Algorithms and Applications by John G. Proakis & D.G. Manolakis, Prentice Hall, 1997. (Unit II, Unit III, Unit IV, Unit V)

3. Digital Signal Processing by S. K. Mitra, 3rd edition, McGraw-Hill, 2007. (Unit V)

Reference Books:

1. Signals and Systems by A. V. Oppenheim, A. S. Willsky & S. H. NAWAB, 2nd edition, Prentice Hall, 1996.

2. Digital Signal Processing by S. Salivahanan, A. Vallavaraj, C. Gnanapriya, Tata McGraw-Hill, 2000.

3. Digital Signal Processing by A. Anand Kumar, PHI Learning Pvt. Ltd, 2012.

Course Outcomes:

At the end of the course student will get the ability to

- Synthesize discrete time signals from analog signal.
- Use time domain and frequency domain analysis tools.
- Apply forward and Reverse Transformation.
- Visualize various applications of DSP and explore further possibilities.
- Design IIR and FIR filters

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: VI

Subject: **VLSI Design lab** Code: **C028621(028)**

Total Lab Periods: 36 Batch Size: 30
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To Study Architecture of CPLD
2. To Study Architecture of FPGA
3. To Design Half Adder in Data Flow Style of Modeling and Implement it in the CPLD.
4. To Design Full Adder in Structural Style of Modeling and Implement it in the FPGA.
5. To Design 4:1 Multiplexer in Behavioral Modeling and Implementation in CPLD.
6. To Design 16:1 Multiplexer using Generate statement and Implementation in FPGA.
7. To Design 8bit adder using Generic statement and Implementation in CPLD.
8. To Design D Flip-Flop in Behavioral Modeling.
9. To Design Sequence Detector using Moore Machine in Behavioral Modeling.
10. To Design Serial Adder using Mealy Machine in Behavioral Modeling.
11. To Prepare and Verify the Layout for NOT Gate.
12. To Prepare and Verify the Layout for NAND Gate.
13. To Prepare and Verify the Layout for NOR Gate.
14. To Prepare the Layout for D-FF.
15. To Prepare the Layout for the logic equation (a * (b+c))'

EDA Tools to be used:

Front End: Modelsim, FPGA Advantage, Xilinx, EdWinXP, Active HDL.

Back End: Cadence, Zeni-EDA, Calibre, Tanner, Synopsis, H-Spice

CPLD: XC9572, XC95108.FPGA:XC3S400

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: VI

Subject: **Digital Signal Processing Laboratory** Code: **C028622(028)**
Total Lab Periods: 36 Batch Size: 30
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To generate the basic Analog and Discrete Signals.
2. Implementation of Linear convolution, Circular convolution, linear convolution using circular convolution.
3. DFT Implementation for a given signal.
4. To plot Fourier Transform amplitude spectrum and phase spectrum for a given function.
5. To plot frequency response in Z-domain for the given transfer function.
6. To plot frequency response in S-domain for a given transfer function.
7. To plot Fast Fourier Transform (amplitude & phase).
8. To sample a sinusoidal signal at Nyquist rate, above the Nyquist Rate and below the Nyquist Rate.
9. Design & implementation of IIR filters[LPF,HPF,BPF,BSF].
10. Design & implementation of FIR filters[LPF,HPF,BPF,BSF].
11. To design various filters using Simulink.
12. To design a Graphical User Interface to display various basic signals [sinewave ,sinc wave, etc].
13. To perform Interpolation and decimation [Multirate DSP].
14. To design a digital notch filter and embed it on a digital signal processor block.
15. Experiments with application of DSP in Communication / Speech Processing / Image Processing.

(Institutes may append more programmes / Experiments based on the infrastructure available)

List of Equipments /Machine Required:

C++Compiler, Simulation Software, DSP Processor kit, Digital Storage CRO, Spectrum Analyzer.

Recommended Books:

1. Digital Signal Processing, Vallavaraj, Salivahanan, Gnanapriya, TMH
2. Stein, J. Digital Signal Processing-a computer science perspective. Wiley

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: VI

Subject: **Machine Learning Lab** Code: **C028623(028)**
Total Lab Periods: 36 Batch Size: 30
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. Heuristics and search strategy for Travelling sales person problem.
2. Implement n-queens problem using Hill-climbing, simulated annealing, etc.
3. Tic-tac-toe game simulation using search and heuristics.
4. Solve 3-SAT, 3-CNF algorithms using agents.
5. Describe the Sudoku game and represent the actions using First-order / Propositional logic.
6. Sorting algorithms employing forward chaining.
7. Logical reasoning examples for E-commerce stores using forward/backward chaining.
8. Study of Machine learning tool.
9. Exercises on decision trees, SVM using the tool.
10. K-means clustering implementation using tool.
11. Agglomerative, divisive, fuzzy clustering using tool.
12. Implement and demonstrate the FIND-S algorithm for finding the most specific hypothesis based on a given set of training data samples.
13. For a given set of training data examples stored in a .CSV file, implement and demonstrate the Candidate-Elimination algorithm to output a description of the set of all hypotheses consistent with the training examples.
14. Write a program to demonstrate the working of the decision tree based ID3 algorithm.
15. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.
16. Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets.
17. Write a program to implement the naïve Bayesian classifier for a sample training data set stored as a .CSV file.
18. Compute the accuracy of the classifier, considering few test data sets.
19. Assuming a set of documents that need to be classified, use the naïve Bayesian Classifier model to perform this task. Calculate the accuracy, precision, and recall for your data set.
20. Write a program to construct a Bayesian network considering medical data. Use this model to demonstrate the diagnosis of heart patients using standard Heart Disease Data Set. Apply EM algorithm to cluster a set of data stored in a .CSV file.
21. Use the same data set for clustering using k-Means algorithm. Compare the results of these two algorithms and comment on the quality of clustering.
22. Write a program to implement k-Nearest Neighbor algorithm to classify the iris data set. Print both correct and wrong predictions.
23. Implement the non-parametric Locally Weighted Regression algorithm in order to fit data points. Select appropriate data set for your experiment and draw graphs.

Requirements:

Java/Python ML library classes/API etc.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of Technology

Branch: Electronics & Telecommunication

Semester: VI

Subject: **Soft Computing lab** Code: **C028624(028)**
Total Lab Periods: 36 Batch Size: 30
Maximum Marks: 40 Minimum Marks: 20

List of Experiments: (At least Ten experiments are to be performed by each student)

1. To design, implement and simulate the combinational logic circuit for the function f{A,B,C) = ∑(0,4,5,8,II,I5) + d (1)
2. To design, implement and simulate the Full adder using two half adder.
3. To design, implement and simulate the 8 bit adder using Full adder.
4. To design, implement and simulate the 3 : 8 Decoder.
5. To design, implement and simulate the 16 : 1 Multiplexer using 4 : 1 Multiplexer.
6. To design, implement and simulate the Binary to BCD code Converter by Showing BCD No. on7segment Display.
7. To design, implement and simulate the Look ahead carry.
8. To design, implement and simulate the Flip-Flop.
9. To design, implement and simulate the Ring Counter.
10. To design, implement and simulate the Decade counter using D-Flip-Flop.
11. To design, implement and simulate the Divide by 32 (+32) digital logic by counter and flip-flop.
12. To design, implement and simulate the Hamming code converter.
13. To design, implement and simulate the 4 bit comparator.
14. To design, implement and simulate the Finite State Machine by Moore method.
15. To design, implement and simulate the Finite State Machine by Mealy circuit.
16. To design, implement and simulate the Digital clock.
17. Design and simulation of rectifiers. a) Half-wave rectifier b) Half-wave rectifier with capacitor filter. c) Full-wave rectifier d) Bridge rectifier.
18. Plot the output response of clipper and clamper circuits a) Positive clipper. b) Negative clipper c) Combination clipper d) Clamper
19. Design and simulation of RC phase shift oscillator
20. Plot output response of following op-amp based circuits a) inverting and non-inverting amplifier. b) integrator. c) differentiator.

21. Design and simulation of static CMOS logic circuits a) Inverter b) NAND gate c) NOR gate

22. Plot the output response of a level triggered and edge triggered D- Flip-Flops.

23. Extract parasitic capacitances of NMOS and PMOS transistors.

24. Study the impact of channel length, width and power supply variations on rise time and fall time of an inverter. Further, investigate the impact of these parameters on static and dynamic power.

25. Perform transient and ac analysis of CE amplifier and plot the magnitude and phase response

List of Equipments/Machine Required:

PCs with simulation software like SPICE, MULTISIM, COMSIM, MATLAB, TINA PRO installed

Recommended Books:

D. V. Bout : The Practical Digital Circuit Designer Lab Book ; Prentice-Hall., 1999.

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Program / Semester: **B.Tech (VI)**	Branch: **Humanities**
Subject: **Technical Communication & Soft Skills**	Course Code: **C000601(046)**
Total Marks (Internal Assessment): 10	L: 0 T:0 P: 2 Credit(s): 0
Internal Assessments to be conducted: 02	Duration (End Semester Exam): **NA**

UNIT-1 Communication Skills-Basics: Understanding the communicative environment, Verbal Communication; Non Verbal Communication & Cross Cultural Communication, Body Language & Listening Skills; Employment Communication &writing CVs, Cover Letters for correspondence. Common errors during communication, Humour in Communication.

UNIT-2 Interpersonal communication: Presentation, Interaction and Feedbacks, Stage Manners, Group Discussions (GDs) and facing Personal Interviews, Building Relationships, Understanding Group Dynamics- I, Emotional and Social Skills, Groups, Conflicts and their Resolution, Social Network, Media and Extending Our Identities.

UNIT- 3 Vocational skills: Managing time: Planning and Goalsetting, managing stress: Types of Stress; Making best out of Stress, Resilience, Work-life balance, Applying soft-skills to workplace.

UNIT-4 Mindsets and Handling People: Definitions and types of Mindset, Learning Mindset, Developing Growth Mindset, Types of People, How to Lead a Meeting, How to Speak Effectively in Meetings, Behavior & Roles in Meetings, Role Play: Meeting.On Saying "Please", How to say "NO".

UNIT-5Positive Pschycology: Motivating oneself, Persuasion, Survival Strategies, Negotiation, Leadership and motivating others**,** controlling anger**,** Gaining Power from Positive Thinking.

Text Books:

1. Petes S. J., Francis. Soft Skills and Professional Communication. New Delhi: Tata McGraw-Hill Education, 2011.
2. Stein, Steven J. & Howard E. Book. The EQ Edge: Emotional Intelligence and Your Success. Canada: Wiley & Sons, 2006.
3. Dorch, Patricia. What Are Soft Skills? New York: Execu Dress Publisher, 2013.

Reference Books:

- Kamin, Maxine. Soft Skills Revolution: A Guide for Connecting with Compassion for Trainers, Teams, and Leaders. Washington, DC: Pfeiffer & Company, 2013.
- Peale Norman Vincent. The Power of Positive Thinking: 10 Traits for Maximum Result. Paperback Publication. 2011.
- Klaus, Peggy, Jane Rohman & amp; Molly Hamaker. The Hard Truth about Soft Skills. London: Harper Collins E-books, 2007.

Course Outcomes

1. Learn to listen actively to analyse audience and tailor the delivery accordingly.
2. Increase their awareness of communication behaviour by using propriety-profiling tool.
3. Master three "As" of stressful situation: Avoid, Alter, Accept; to cope with stressors and create a plan to reduce or eliminate them.
4. Develop growth mind-set and able to handle difficult person and situations successfully.
5. Develop technique of turning negativity into positivity and generate self-motivation skills.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Information Theory and coding** Code: **C028631(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

- To understand the role of information theory and coding for an efficient, error-free and secure delivery of information using binary data streams.

UNIT I Source Coding: Introduction to Information Theory, Uncertainty and Information, Average Mutual Information, Discrete Memory less Source ,Entropy of Binary Memory Less source and its extension to Discrete Memory Less Source, ,Information Rate, Information Measures for Continuous Random Variables, Kraft Inequality, Rate Distortion Function, Source Coding Theorem, Shannon Fano coding, Huffman coding, The Lempel-Ziv algorithm, Run Length Encoding and the PCX Format, Introduction to JPEG Standard for Lossless and Lossy Compression.

UNIT II Channel Capacity and Coding: Channel Models, Channel Capacity ,Discrete Memory less Channel: Lossless Channel, Deterministic Channel, Noiseless Channel, Binary Symmetric Channel, Binary Erasure Channel, Channel Coding Theorem, Information Capacity Theorem, Shannon's Limit, Gaussian Channel, Parallel Gaussian Channel

Unit III Error Control Coding (Block codes and Cyclic Codes): Linear Block Codes for Error Correction & Cyclic Codes: Introduction to Error Correcting Codes, Basic Definitions, properties of Linear Block Codes ,Matrix Description of Linear Block Codes, Equivalent Codes, Parity Check Matrix, Decoding of a Linear Block Code, Syndrome Decoding, Hamming Codes. Cyclic Codes: Polynomials, The Division algorithm for Polynomials, Encoding and Decoding of Cyclic Codes, Matrix Description of cyclic codes.

UNIT IV Error Control Coding (Convolutional Codes) : Convolutional Codes: Introduction to Convolutional Codes, Tree codes and Trellis Codes, Polynomial Description of Convolutional Codes (analytical Representation),Graphical Representation: The State diagram, Code Trellis and Code Tree , Distance Notions for Convolutional Codes, The Generating Function, Matrix Description of Convolutional Codes, Viterbi Decoding.

UNIT V Error Control Coding(TCM,BCH codes and LDPC codes): Introduction to TCM:TCM Encoder, Mapping by Set Partitioning, Ungerboeck's TCM Design Rules. Bose-Chaudhuri-Hocquenghem (BCH) Codes: Introduction to BCH Codes, Primitive Elements, Minimal Polynomials, Generator Polynomials in Terms of Minimal Polynomials, Generation of BCH Codes, Decoding of single error in BCH Codes, Introduction to LDPC codes, Representation of LDPC codes using Tanner graph.

Text Books:

1. Information Theory coding & Cryptography by Ranjan Bose,(Unit- I,II,III,IV,V) ,3rd Ed.,Tata McGraw-Hill.

2. Communication Systems, Simon Haykin, Wiley India.

Reference Books:

1. Principles of Digital Communication - Das MullickChatterjee, Willey Eastern Publications
2. Digital communication –B.Sklar, Pearson Publication
3. Digital communication - Prokais, Tata McGrawHill
4. Channel Codes – Classical and Modern, William Ryan, Shu Lin, CUP, 2009.

Course Outcomes

1. Students will be able to analyze source coding techniques like the Huffman encoding, Shannon Fano encoding , Lempel Ziv encoding and Run Length encoding.
2. Students will be able to categorize different types of channels and can determine capacity of a given channel.
3. Students will be able to encode and decode using Block codes and Cyclic codes
4. Students will be able to use graphical method ,polynomial and polynomial matrix to describe convolutional codes.
5. Students will be able to use the mathematical tools developed including primitive element to study BCH codes, and can draw tanner graph of LDPC codes.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Microelectronics Technology** Code: **C028632(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:
1. To get and overview of the field of integrated circuit design.
2. To understand various oxidation techniques.
3. To understand diffusion and ion implantation methods.
4. To understand steps of wafer preparation.
5. To understand MOSFET technology.

UNIT – I Introduction: The Historical Prospect of Integrated Circuits, Silicon Wafers, Wafer Terminology. Crystal Growth: The Czochralski Technique, Bridgeman Technique, Float Zone Process.

UNIT – II Oxidation: Thermal Oxidation, Kinetics of Thermal Oxidation, Film Deposition, Dielectric Deposition, Polysilicon Deposition.

UNIT – III Diffusion: Diffusion Mechanics, Diffusion Equation, Diffusion Profile. Ion Implantation: Implantation Mechanism, Ion Implantation System, Low Energy Implantation, High Energy Implantation.

UNIT – IV Epitaxy: Vapor Phase Epitaxy, Liquid Phase Epitaxy, Molecular Beam Epitaxy. Lithography: Optical Lithography, Electron Beam Lithography, X-Ray Lithography, Ion Beam Lithography. Etching: Wet Chemical Etching, Reactive Chemical Etching. Metallization: Physical Vapor deposition, Chemical Vapour deposition, Aluminum Metallization, Metallization with Silicides. Process Simulation and Integration

UNIT – V MOSFET Technology: Introduction, MOS Structure. MOS Transistor: MOSFET Structure, Enhancement MOSFET, Threshold Voltage, Depletion MOSFET, Operation of MOSFET. MOSFET Characteristics: Gradual Channel Approximation, Charge Control Model, Velocity Saturation Effects, Channel Length Modulation, Subthreshold region. MOS Capacitance and Equivalent Circuit. Scaling of MOSFET: Short channel Effects, SPICE model for MOSFETs. MOSFET Fabrication.

Text Book:

1. VLSI Design by Sujata Pandey & Manoj Pandey, Dhanpat Rai & co.

2. VLSI Technology by S.M. Sze, TMH Book Company

Reference Book:

1. VLSI Fabrication Principles by Sorab K. Gandhi, Wiley & Sons, New York.

2. Physics & Technology of Semiconductor Devices by A.S. Grove, Wiley & Sons, New York.

Course Outcomes

1. Student gets brief historical overview specific to VLSI design field.

2. Student learns about oxidation techniques.

3. Student gets an insight into diffusion and ion implantation mechanism.

4. Student is able to understand different steps of wafer preparation.

5. Student gets an overview of microelectronics devices and MOSFET technology.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **ARM System Architecture & Design** Code: **C028633(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

The objective of this course is to give the students a thorough exposure to ARM architecture and make the students to learn the ARM programming & Thumb programming models.

UNIT I ARCHITECTURAL FEATURES OF ARM PROCESSOR: Processor modes, Register organization, Exceptions and its handling, Memory and memory-mapped I/Os, ARM and THUMB instruction sets, addressing modes, ARM floating point architecture and DSP extensions, ARM co-processors.

UNIT II ARM 9 TDMI ARCHITECTURAL STUDY: H/W architecture, Timing diagrams for various accesses, Memory buses: AMBA, ASB, APB, Case study of Intel Xscale architecture or Samsung ARM implementations

UNIT III ARM AND THUMB INSTRUCTION SETS: Conditional execution and flags, Branch instructions, The barrel shifter, Immediate constants, Single register data transfer, Block data transfer, Stack management, Coprocessor instructions, Register access in Thumb, ARM architecture V5TE new instructions, Assembler workbooks ARM / THUMB INTERWORKING: Switching between states, Branch exchange example, Mixing ARM and Thumb subroutines, ARM to thumb veneer, Thumb-to-ARM veneer, Interworking calls, and Interworking using codewarrior.

UNIT IV ARM DEVELOPPER SUITE (ADS) OVERVIEW: Using the core tools, C/C++ compilers key features, Supplied libraries, Code warrior introduction, Debugging with multi-ICE.
ADS INTRODUCTORY WORKBOOK: Compiling and running an example, Creating a header file, Creating a new project, Viewing registers and memory. E
XCEPTION HANDLING: Exception return instructions, Exception priority, Vector table instructions, Chaining exception handlers, Register usage in exception handlers, FIQ vs IRQ, Example C interrupt handler, Software managed interrupt controller, Issues when re-enabling interrupts, C nested interrupt example, Invoking SWIs, Data abort with memory management, The return address

UNIT V EMBEDDED SOFWARE DEVELOPMENT: ROM or RAM at 0x0, ROM/RAM remapping, Exception vector table, Reset handler, Initialization : stack pointers, code and data areas, C library initialization, Scatter loading, Linker placement rules, Long branch veneers, C library functionality, Placing the stack and heap, Debugging ROM images.

Text Books:

1. ARM System Developer's Guide: Designing and Optimizing, Sloss Andrew N, Symes Dominic, Wright Chris, Morgan Kaufman Publication.
2. ARM System-on-Chip Architecture, Steven Furber, Pearson Education

Reference Books:

1. Technical references on www.arm.com.
2. Technical reference manual for ARM processor cores, including Cortex, ARM 11, ARM 9 & ARM 7 processor families.
3. User guides and reference manuals for ARM software development and modeling tools.
4. David Seal, ARM Architecture Reference Manual, Addison-Wesley.

Course Outcomes

Students are able to

- Describe the programmer's model of ARM processor and create and test assembly level programming.
- Analyze various types of coprocessors and design suitable co-processor interface to ARM processor.
- Analyze floating point processor architecture and its architectural support for higher level language.
- Become aware of the Thumb mode of operation of ARM.
- Identify the architectural support of ARM for operating system and analyze the function of memory Management unit of ARM.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Image Processing & remote sensing** Code: **C028634(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To know the basic components of an image processing system..
2. To understand the basics of the human visual system as they relate to image processing including spatial frequency resolution and brightness adaptation.
3. To teach the students about various image enhancement techniques and transformation of images.
4. To have an illustrative idea about various edge detection techniques.
5. To give knowledge about the need of thresholding and types of thresholding techniques.
6. To have a brief idea about approaches to restoration and image compressions

Unit – I: Introduction and Basic Concepts: Introduction, Basic Concepts of remote sensing, Airborne and space-borne sensors, Passive and active remote sensing, EMR Spectrum, Energy sources and radiation principles. Energy Interactions in the atmosphere. Energy interactions with earth surface features, Spectral reflectance curves , Energy interactions with earth surface features.

Unit – II: Remote Sensing System : Satellites and orbits, Geo-Synchronous, sun synchronous and polar orbiting satellites, Spatial, Spectral and radiometric resolutions, Temporal resolution, Spatial, Spectral and radiometric resolutions, Multispectral, thermal and hyper spectral remote sensing. Remote sensing satellites and their features.

Unit – III : Digital Image Processing – Image Restoration: Geometric Corrections, Ground Control Points (GCP), Co-registration of data, Atmospheric corrections, solar illumination correction.

Unit – IV: Digital Image Processing – Image Enhancement: Concept of Color, RGB and HIS color schemes, Color composites. Contrast stretching – linear and non-linear stretching. Filtering techniques, Edge enhancement, Density slicing, Thresholding, Intensity-Hue-Saturation (HIS) images, Time Composite images, Synergetic images.

Unit – V: Digital Image Processing – Information Extraction: Supervised and unsupervised classification, Fuzzy classification, Image transformations, Ratio images, Vegetation Indices, Principal component analysis.

Text Books:

1. Digital Image Processing by Gonzalez & Woods, Pearson Education.
2. Introduction to Digital Image Processing by Alasdair Mc Andrew, Cengage learning.
3. Fundamental of Digital Image Processing by AK Jain, PHI.
4. Joseph, G. (2004): Fundamentals of Remote Sensing, Universities Press, Hyderabad, India
5. Lillesand, T. M., Kiefer, R. W. and Chipman, J. W. (2008): Remote Sensing and Image Interpretation, John Wiley & Sons, New Delhi

Reference Book:

1. Image Processing, Analysis and Machine Vision by Milan Sonka,T homson Learning.
2. Digital Image Processing by Pratt W.K, John Wiley & Sons.
3. Digital Image Processing by Madhuri A. Joshi, PHI
4. Sabins, F. F. (1996): Remote Sensing: Principles and Interpretation, W. H. Freeman and Company, San Francisco
5. Jensen, J. R. (2005): Introductory Digital Image Processing, Prentice Hall, New Jersey
6. Campbell, J. (2002): Introduction to Remote Sensing, Taylor & Francis, London

Course Outcomes:

1. Students will understand the basic concepts of image and remote sensing.
2. Emphasis will be to develop engineering skills and intuitive understanding of the tools used in Image Processing.
3. Students will be able to do various operations on images like Image enhancement, transformation, sharpening etc.
4. Students can analyze various edge detection techniques and their algorithms.
5. Students will be able to use various thresholding techniques and segmentations.
6. Students will be able to visualize approaches used in image restoration.

Chhattisgarh Swami Vivekananda Technical University, Bhilai
Name of program: Bachelor of Technology
Branch: Electronics & Telecommunication
Semester: VI

Subject: **Wireless Sensor Networks** Code: **C028635(028)**
Total Theory Periods: 40 Class Tests: Two (Minimum)
Total Tutorial Periods: 10 Assignments: Two (Minimum)
ESE duration: Three Hours Maximum Marks: 100 Minimum Marks: 35

Course Objectives:

1. To understand the WSN node Architecture and Network Architecture
2. To identify the Wireless Sensor Network Platforms
3. To program WSN using embedded C
4. To design and Develop wireless sensor node

UNIT I: Introduction to wireless sensor networks (WSN), Hardware of wireless sensor node, Network deployment, Localization, Coarse grained and fine grained localization, Network wide localization, Theoretical analysis of localization techniques.

UNIT II: Time synchronization, Traditional approaches, Fine grained clock synchronization, Coarse grained data synchronization. Medium access and sleep scheduling.

UNIT III: Sleep based topology control, Topologies for connectivity, topologies for coverage, Cross layer issues. Energy efficient and robust routing, Metric based approaches, Routing with diversity, Multipath routing, Energy aware routing.

UNIT IV: Distributed detection and estimation in sensor networks.

UNIT V: Data centric networking, Data centric routing, Data gathering with compression, Querying, Data centric storage and retrieval.

Text Books:

1. Networking wireless sensor nodes, B Krishnamachari, Cambridge University Press, New York 2005.

2. Wireless sensor networks: An information processing approach, F Zhao, L J Guibas, Morgan Kaufman Publishers/ Elsevier, New Delhi 2004.

Reference Books

1. Sabrie Soloman, SENSORS HANDBOOK by Mc Graw Hill publication.

2. Feng Zhao, Leonidas Guibas, Wireless Sensor Networks, Elsevier Publications.

3. Kazem Sohrby, Daniel Minoli, Wireless Sensor Networks: Technology, Protocols and Applications, Wiley-Inderscience

4. Philip Levis, And David Gay Tinyos Programming by Cambridge University Press.

Course Outcomes:

After completing this course the students should:

1. Understand and explain common wireless sensor node architectures.
2. Be able to carry out simple analysis and planning of WSNs.
3. Demonstrate knowledge of MAC protocols developed for WSN.
4. Demonstrate knowledge of routing protocols developed for WSN.
5. Understand and explain mobile data-centric networking principles.
6. Be familiar with WSN standards.