

Chhattisgarh Swami Vivekanand Technical University, Bhilai

SCHEME OF EXAMINATION

M.E. Electronics & Telecommunication (Specialization in VLSI Design)

FIRST SEMESTER

Sr No	Board of Study	Subject Code	Subject	Periods Per Week			Scheme of Examination			Total Marks	Credit L+(T+P) /2
				L	T	P	Theory / Practical				
							ESE	CT	TA		
1	Electronics & Telecom	560111 (28)	VLSI Technology	3	1	-	100	20	20	140	4
2	Electronics & Telecom	560112 (28)	VLSI System Design	3	1	-	100	20	20	140	4
3	Electronics & Telecom	560113 (28)	MOS Circuit Design	3	1	-	100	20	20	140	4
4	Electronics & Telecom	560114 (28)	Modelling with HDLs	3	1	-	100	20	20	140	4
5	Refer Table 1		Elective – I	3	1	-	100	20	20	140	4
6	Electronics & Telecom	560121 (28)	VHDL Modelling Laboratory	-	-	3	75	-	75	150	2
7	Electronics & Telecom	560122 (28)	Computer Simulation Laboratory	-	-	3	75	-	75	150	2
TOTAL				15	5	6	650	100	250	1000	24

Table-I

Elective-I			
Sr. No.	Board of Study	Subject Code	Subject
1	Electronics & Telecom	560131 (28)	CMOS RF Circuit Design
2	Electronics & Telecom	560132 (28)	Real Time System & Software
3	Electronics & Telecom	560133 (28)	Digital Image Processing

L - Lecture
P - Practical
CT - Class Test

T - Tutorial
ESC – End Semester Exam
TA – Teachers Assessment

Note (1) – 1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session .

Note (2) – Choice of elective course once made for an examination cannot be changed in future examinations.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester : **M. E. – I**

Branch: **Electronics & Telecommunication**

Subject : **VLSI Technology**

Code: **560111 (28)**

Total Theory Periods : **40**

Total Tutorial Periods : **12**

Total Marks in End Semester Examination: **100**

Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

Crystal growth & wafer preparation. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc. Vapors phase Epitaxy Basic Transport processes & reaction kinetics, doping & auto doping, equipments, & safety considerations, buried layers, epitaxial defects, molecular beam epitaxy, equipment used, film characteristics, SOI structure.

UNIT 2

Growth mechanism & kinetics, Silicon oxidation model, interface considerations, orientation dependence of oxidation rates thin oxides. Oxides. Oxidation technique & systems dry & wet oxidation. Masking properties of SiO₂.

UNIT 3

Diffusion from a chemical source in vapor form at high temperature, diffusion from doped oxide source, diffusion from an ion implanted layer.

UNIT 4

Optical Lithography: optical resists, contact & proximity printing, projection printing, electron lithography: resists, mask generation. Electron optics: raster scans & vector scans, variable beam shape. X-ray lithography: resists & printing, X ray sources & masks. Ion lithography.

UNIT 5

Reactive plasma etching, AC & DC plasma excitation, plasma properties, chemistry & surface interactions, feature size control & anisotropic etching, ion enhanced & induced etching, properties of etch processing. Reactive Ion Beam etching, Specific etches processes: poly/polycide. Trench etching,

Text:

1. S. M. Sze, "VLSI Technology", McGraw Hill Book Co.
2. S.K.Gandhi, "VLSI Fabrication Principles", John Wiley and Sons, NY.

References:

1. Chen, "VLSI Technology" Wiley, March.
2. D.Nagchoudhary, "Principles of Microelectronics Technology", Wheeler (India).

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester: **M. E. – I**
Subject: **VLSI System Design**
Total Theory Periods: **40**

Branch: **Electronics & Telecommunication**
Code: **560112 (28)**
Total Tutorial Periods: **12**

Total Marks in End Semester Examination: **100**
Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

VLSI System Design methodology: Structure Design, Strategy, Hierarchy, Regularity, Modularity, Locality. System on Chip Design options: Programmable logic and structures, Programmable interconnect, programmable gate arrays, Sea of gate and gate array design, standard cell design, full custom mask design.

UNIT 2

Chip Design Methods : Behavioral synthesis, RTL synthesis, Logic optimization and structural tools layout synthesis, layout synthesis, EDA Tools for System

Design capture tools: HDL Design, Schematic Design, Layout Design, Floor planning and Chip Composition. Design Verification Tools: Simulation Timing Verifiers, Net List Comparison Layout Extraction, Design Rule Verification.

UNIT 3

Data Path Sub System Design: Introduction, Addition, Subtraction, Comparators, Counters, Boolean logical operations, coding, shifters, Multiplication, Parallel Prefix computations.

Array Subsystem Design: SRAM, Special purpose RAMs, DRAM, Read only memory, Content Addressable memory, Programmable logic arrays.

Control Unit Design: Finite State Machine (FSM) Design, Control Logic Implementation: PLA control implementation, ROM control implementation.

UNIT 4

CMOS Subsystem Design: Basic theory of CMOS (detail) – Data path operations –Parity generator – Comparators – Zero/one detectors- Binary counters – Boolean operations – Multiplication – Shifters.

UNIT 5

Memory Elements: Read/write memory: - RAM- Register files – FIFOs, LIFOs, SIPOs- Serial Access memory. Read only memory – Content Addressable memory - Finite – State Machine – FSM Design procedure – Control Logic implementation: - PLA Control implementation – ROM Control implementation – Multilevel logic – An example of control logic implementation.

Text:

1. N.H.E.Weste and K.Eshraghian, “ Principles of CMOS VLSI Design”, 2nd Edition - Addison Wesley,1993.
2. Jan .M.Rabaey, “Digital Integrated Circuits a design perspective” , PHI 1st Edition, 1995.

Reference:

Weste and Eshraghian, “Principles of CMOS VLSI design” Addison-Wesley, 2002
“CMOS VLSI Design” by Wolf pearson

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester: **M. E. – I**
Subject: **MOS Circuit Design**
Total Theory Periods: **40**
Total Marks in End Semester Examination: **100**
Minimum No. of Class Tests to be Conducted: **02**

Branch: **Electronics & Telecommunication**
Code: 560113 (28)
Total Tutorial Periods : **12**

UNIT 1

Introduction:

Basic principle of MOS transistor, Introduction to large signal MOS models (long channel) for digital design. **The MOS Inverter:** Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption.

UNIT 2

MOS Circuit Layout & Simulation: MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation

UNIT 3

Combinational MOS Logic Design

Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits.

Dynamic MOS design: Dynamic logic families and performances.

UNIT 4

Sequential MOS Logic Design

Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design

Interconnect & Clock Distribution

Interconnect delays, Cross Talks, Clock Distribution. Introduction to low power design, Input and Output Interface circuits.

UNIT 5

BiCMOS Logic Circuits

Introduction, BJT Structure & operation, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits, BiCMOS Applications

Text:

1. Kang & Leblebici "CMOS Digital IC Circuit Analysis & Design"- McGraw Hill, 2003
2. Rabey, "Digital Integrated Circuits Design", Pearson Education, Second Edition, 2003

Reference:

1. Weste and Eshraghian, "Principles of CMOS VLSI design" Addison-Wesley, 2002
2. "CMOS VLSI Design" by Wolf pearson

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester : **M. E. – I**

Subject : **Modelling With HDLs**

Total Theory Periods : **40**

Total Marks in End Semester Examination: **100**

Minimum No. of Class Tests to be Conducted: **02**

Branch: **Electronics & Telecommunication**

Code: 560114 (28)

Total Tutorial Periods : **12**

UNIT 1

Introduction to PLDs & FPGAs : ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array (LCA) – I/O Block – Programmable interconnect – Xilinx – 3000 series and 4000 series FPGAs. Altera CPLDs, altera FLEX 10K series PLDs.

UNIT 2

Placement and routing : Mincut based placement – iterative improvement placement– Routing: Segmented channel routing – Maze routing – Routability and routing resources – Net delays.

UNIT 3

Introduction to VHDL : Digital system design process – Hardware simulation – Levels of abstraction – VHDL requirements – Elements of VHDL – Top down design VHDL operators – Timing – Concurrency – Objects and classes – Signal assignments – Concurrent and sequential assignments.

UNIT 4

Structural, Data flow & Behavioral description of hardware in VHDL: Parts library – Wiring of primitives – Wiring of iterative networks – Modeling a test bench – Top down wiring components – Subprograms. Multiplexing and data selection – State machine descriptions – Open collector gates – Three state bussing. - Process statement – Assertion statement – Sequential wait statements – Formatted ASCII I/O operations MSI based design.

UNIT 5

Introduction to Verilog HDL : Lexical conventions – Data types – System tasks and Compiler Directives- Modules and Ports- Gate Level Modeling with Examples.

Text:

P.K. Chan & S. Mourad, “Digital Design sing Field Programmable Gate Array” 1st Edition, Prentice Hall, 1994.

J. V. Old Field & R.C. Dorf, “ Field Programmable Gate Array”, John Wiley, 1995.

References:

1. M. Bolton, “ Digital System Design with Programmable Logic”, Addison Wesley, 1990.
2. Thomas E. Dillinger, “ VLSI Engineering”, Prentice Hall, 1st Edition, 1998.
3. Douglas Perry, “VHDL”, 3rd Edition, McGraw Hill 2001.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester: **M. E. – I**

Subject: **CMOS RF Circuit Design**

Total Theory Periods: **40**

Total Marks in End Semester Examination: **100**

Minimum No. of Class Tests to be Conducted: **02**

Branch: **Electronics & Telecommunication**

Code: 560131 (28)

Total Tutorial Periods: **12**

UNIT 1

Introduction to RF design and Wireless Technology: Importance of Radio frequency Design, Dimensions and Units, Frequency Spectrum, RF behavior of Passive Component, High-frequency resistor, High-frequency capacitors, High-frequency inductors, Chip Components and circuit board Considerations, Chip resistors, Chip capacitors, Surface-mounted inductors.

UNIT 2

Single and Multiport Networks: Basic definitions interconnecting networks, Series connection of networks , Parallel connection of networks , Cascading of networks, Summary of ABCD network representations , Network properties and applications , Interrelation between parameter sets , Analysis of microwave amplifier , Scattering parameters , Definition of scattering parameters, Meaning of S-Parameters , Chain scattering matrix, Conversion between Z-and S- parameters, Signal flow chart modeling, Generalization of Sparameters, Practical measurements of S-Parameters .

UNIT 3

BJT and MOSFET Behavior at RF Frequencies

BJT and MOSFET behavior at RF frequencies, Modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT 4

RF Circuits Design

Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Linearization techniques, Design issues in integrated RF filters.

UNIT 5

Oscillator and Mixers: Basic oscillator model, Negative resistance oscillator, Feedback oscillator design, Design steps, Quartz oscillators, High frequency oscillator, configuration, Fixed frequency oscillators, Dielectric resonator oscillator, YAGI-tuned oscillator, Voltage control oscillator, GUNN element oscillators, Basic characteristics of mixers, Basic concepts, Frequency domain considerations, Single ended mixers design , Double -Balanced mixer.

Text Book :

1. RF Circuit Design Theory and applications” Reinhold Ludwig Pavel Bretchko.
2. Thomas H. Lee “Design of CMOS RF Integrated Circuits” Cambridge University press 1998.

References:

1. B. Razavi “RF Microelectronics” PHI 1998.
2. R. Jacob Baker, H.W. Li, D.E. Boyce “ CMOS Circuit Design, layout and Simulation” PHI 1998

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester : **M. E. – I**

Branch: **Electronics & Telecommunication**

Subject : **Real Time System & Software**

Total Theory Periods : **40**

Code: **560132 (28)**

Total Marks in End Semester Examination: **100** Total Tutorial Periods : **12**

Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

Introduction, Real-time Versus Conventional Software, Computer Hardware for Monitoring and Control, Software Engineering Issues. Process and State-based Systems model, Periodic and Sporadic Process, Cyclic Executives, CE definitions and Properties, Foreground-Background Organizations, Standard OS and Concurrency – Architectures, Systems Objects and Object-Oriented Structures, Abstract Data Types, General Object Classes

UNIT 2

Requirements and Design Specifications: Classification of Notations, Data Flow Diagrams, Tabular Languages, State Machine, Communicating Real Time State Machine- Basic features, Timing and clocks, Semantics Tools and Extensions, Statecharts-Concepts and Graphical Syntax, Semantics and Tools

Declarative Specifications: Regular Expressions and Extensions, Traditional Logics-Propositional Logic, Predicates, Temporal logic, Real time Logic

Deterministic Scheduling : Assumptions and Candidate Algorithms, Basic RM and EDF Results, Process Interactions-Priority Inversion and Inheritance

UNIT 3

Execution Time Prediction: Measurement of Software by software, Program Analysis with Timing Schema, Schema Concepts, Basic Blocks, Statements and Control, Schema Practice, Prediction by optimisation, System Interference and Architectural Complexities Timer Application, Properties of Real and ideal clocks, Clock Servers – Lamport's Logical clocks, Monotonic Clock service, A software Clock server, Clock Synchronization- Centralized Synchronization, Distributed Synchronization

UNIT 4

Programming Languages: Real Time Language Features, Ada-Core Language, Annex Mechanism for Real Time Programming, Ada and Software Fault Tolerance, Java and Real-time Extensions, CSP and Occam

UNIT 5

Operating Systems: Real Time Functions and Services, OS Architectures-Real Time UNIX and POSIX, Issues in Task management- Processes and Threads, Scheduling, Synchronization and communication

Text Book:

Real – Time Systems and software by Alan C. Shaw ; John Wiley & Sons Inc

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester: **M. E. – I**

Branch: **Electronics & Telecommunication**

Subject: **Digital Image Processing**

Total Theory Periods: **40**

Code: **560133 (28)**

Total Marks in End Semester Examination: **100**

Total Tutorial Periods: **12**

Minimum No. of Class Tests to be Conducted: **02**

UNIT 1

Introduction And Digital Image Fundamentals: Digital Image Representation, Fundamental Steps in Image Processing, Elements of Digital image processing systems, Sampling and quantization, some basic relationships like neighbours, connectivity, Distance measure between pixels, Imaging Geometry.

UNIT 2

Image Transforms: Discrete Fourier Transform, Some properties of the two-dimensional fourier transform, Fast fourier transform, Inverse FFT.

UNIT 3

Image Enhancement: Spatial domain methods, Frequency domain methods, Enhancement by point processing, Spatial filtering, Lowpass filtering, Highpass filtering, Homomorphic filtering, Colour Image Processing.

Image Restoration: Degradation model, Diagonalization of Circulant and Block-Circulant Matrices, Algebraic Approach to Restoration, Inverse filtering, Wiener filter, Constrained Least Square Restoration, Interactive Restoration, Restoration in Spatial Domain.

UNIT 4

Image Compression: Coding, Interpixel and Psychovisual Redundancy, Image Compression models, Error free comparison, Lossy compression, Image compression standards.

Image Segmentation: Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation.

UNIT 5

Representation and Description: Representation schemes like chain coding, Polygonal Approximation, Signatures, Boundary Segments, Skeleton of region, Boundary description, Regional descriptors, Morphology.

Recognition and Interpretation: Elements of Image Analysis, Pattern and Pattern Classes, Decision-Theoretic Methods, Structural Methods, Interpretation.

Text:

1. Rafael C. Gonzalez & Richard E. Woods, "Digital Image Processing", AWL.
2. A.K. Jain, "Fundamental of Digital Image Processing", PHI.

Reference:

1. Rosefield Kak, "Digital Picture Processing",
2. W.K. Pratt, "Digital Image Processing",

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester : **M. E. – I**

Branch: **Electronics & Telecommunication**

Subject : **VHDL Modelling Laboratory**

Total Practical Periods: **40**

Code: **560121 (28)**

Total Marks in End Semester Examination: **75**

List of Experiments using VHDL

- 01 Half adder, Full adder, Subtractor Flip Flops, 4bit comparator.
- 02 Parity generator
- 03 Bit up/down counter with load able count
- 04 Decoder and encoder
- 05 8 bit shift register
- 06 8:1 multiplexer
- 07 Test bench for a full adder
- 08 Barrel shifter
- 09 N by m binary multiplier
- 10 RISC CPU (3bit opcode, 5bit address)

TOOLS:

Xilinx Tools, Cadence Tools, Model SIM, Leonardo Spectrum Tools shall be used.

Chhattisgarh Swami Vivekanand Technical University, Bhilai

Semester: **M. E. – I**

Subject: **Computer Simulation Laboratory**

Total Theory Periods: 40

Total Marks in End Semester Examination: **75**

Branch: **Electronics & Telecommunication**

Code: **560122 (28)**

List of Experiments

1. SPICE simulation of basic analog circuits.
2. Analog Circuit simulation using labview tools
3. Verification of layouts (DRC, LVS)
4. Back annotation

Tools used : Cadence tools, Mentor Graphics tools, lab view tools, multisim,